Remarks

Reconsideration and allowance of the subject patent application are respectfully requested.

No amendments are made to the claims. A Listing of Claims is provided for the Examiner's convenient reference.

Applicants acknowledge with appreciation the indication that claims 13, 15, 24, 26, 36, 38, 41, 42 and 52 contain allowable subject matter.

Claims 1-7, 14, 16-18, 25, 27-30, 37, 39, 43-46, 53 and 54 were rejected under 35 U.S.C. Section 103(a) as allegedly being "obvious" over Chin et al. (U.S. Patent No. 6,202,101) in view of Harriman et al. (U.S. Patent No. 6,092,158).

Applicants respectfully traverse this rejection.

Chin et al. discloses a PCI (peripheral component interface) controller 40, a processor controller 42, a memory controller 44 and an AGP (advanced graphics port) controller 46 embodied within an interface controller 14. See Figures 1 and 2. Memory controller 44 arbitrates among processor writes, processor reads, peripheral (i.e., PCI, AGP and GCI) writes, peripheral reads and refresh. See, Chin et al., col. 8, lines 56-59. Chin et al. is particularly concerned with a processor controller that can dispatch memory-destined request cycles (memory request cycles) concurrently with peripheral-destined request cycles (peripheral request cycles). In this manner, peripheral request cycles can be immediately sent if the peripheral bus is clear or peripheral data is available. See Chin et al., col. 2, lines 53-59.

In addition to the various controllers, interface controller 14 also includes multiple address and data queues 50a-50i. These various queues can be classified as address and data queues or merely data queues depending on the flow direction of information and the controllers being linked by the respective queues. Table 1 of Chin et al. shows the characteristics of the queues shown in Figure 2.

With respect to claim 1, the office action contends that queues 50a, 50c, 50e, 50d, 50g and 50j correspond to the claimed buffer memories. Applicants note that queues 50a, 50c, 50e, 50d, 50g and 50j are part of interface controller 14 (see Chin et al., Figure 2), and are not described or illustrated in Chin et al. as being part of the memory controller 44.

In any event, even if queues 50a, 50c, 50e, 50d, 50g and 50j are viewed as being part of the Chin et al. memory controller, Applicants respectfully submit that Chin et al. fails to disclose or suggest the claimed multiple resource buffer or control circuit.

In particular, claim 1 calls for the memory controller to comprise a multiple resource buffer and the office action identifies memory request queue 68 in Figure 6 of Chin et al. as corresponding to this multiple resource buffer. Applicants traverse this contention.

First, the configuration shown in Figure 6 (including queue 68) is clearly and unambiguously described in Chin et al. as being part of the processor controller 42, not memory controller 44. See, e.g., Chin et al., col. 11, lines 6-10 ("...Processor controller 42 includes an in-order queue 42, a peripheral request queue 66, and memory request queue 68.") (emphasis added). Figure 5 shows details of information which can be stored in queues 64, 66 and 68 (see Chin et al., col. 12, lines 44-45) and Figure 6 is an alternative configuration to that shown in Figure 5 (see Chin et al., col. 13, lines 27-28). Because Chin et al. expressly describes queue 68 as being part of the processor controller, queue 68 cannot constitute the claimed multiple resource buffer which is specified to be part of the memory controller.

Second, memory request queue 68 stores requests "dispatched on the processor bus" (col. 11, lines 12-13), not requests from a plurality of buffer memories each of which is operatively coupled to one of a plurality of resources. Because Chin et al. describes queue 68 as storing requests received from a processor bus, queue 68 cannot constitute the claimed multiple resource buffer which is specified as storing requests for memory access from a plurality of buffer memories for multiple resources.

Moreover, claim 1 calls for a control circuit for controlling the transfer of information from the buffer memories to the multiple resource buffer memory. Because queue 68 of Chin et al. does not receive information from a plurality of buffer memories, Chin et al. neither discloses nor suggests a control circuit involved in transferring information as claimed.

The office action mentions M2P queue 50c and the col. 12, lines 65-67 disclosure of Chin et al. in connection with the claimed control circuit. However, queue 50c temporarily stores data read from main memory. Queue 50c is unrelated to the concept of controlling a transfer of information from buffer memories to a multiple resource buffer as claimed. This can be confirmed by reference to Table I of Chin et al. which shows that M2P queue 50c contains data whose source is the memory 18 and whose destination is processor 12.

The office action also references the col. 13, line 51 – col. 14, line 5 disclosure of Chin et al. in connection with the claimed control circuit. However, this disclosure is likewise unrelated to the claimed control circuit. Instead, this disclosure describes queues within processor controller 42 – queues that involve requests from the processor bus, not from a plurality of buffer memories each of which is operatively coupled to one of a plurality of resources requesting memory access.

In addition to the above-noted deficiencies, Chin et al. fails to disclose any control circuit that is operable to control the transfer of information from a plurality of buffer memories to a multiple resource buffer memory to reduce the frequency of switching from main memory write operations to main memory read operations.

The office action cites Harriman et al. for its reference to the grouping of reads and writes in order to "reduce turnaround." Harriman et al., col. 1, lines 43-47.

Applicants respectfully submit that Harriman et al. does not remedy the deficiencies of Chin et al. discussed above with respect to the claimed buffer memories, multiple resource buffer memory and/or control circuit. As such, even assuming for the sake of argument that Harriman et al.'s technique of reducing turnaround is viewed as reducing the switching frequency of main memory read and write operations and this technique were forcibly combined with Chin et al., the subject matter of claim 1 could still not possibly result.

For at least these reasons, Applicants respectfully submit that the subject matter of claim 1 and its dependent claims 2-7 and 14 would not have been made obvious by the proposed combination of Chin et al. and Harriman et al.

These dependent claims contain features that provide additional bases for patentability.

By way of example, claim 14 requires that a resource that is writing to main memory generates a flush signal for initiating the flushing of that resource's write request queue. The office action contends that the "de-queuing" described at col. 13, lines 1-11 of Chin et al. discloses this feature. However, this de-queuing operation is for queue 50c, which contains data whose source is the memory and whose destination is the processor. This queue is not a write request queue and there is no disclosure or suggestion in Chin et al. of initiating the flushing of a resource's write request queue when that resource is writing to main memory. For this additional and independent reason, claim 14 is believed to distinguish over the proposed combination of Chin et al. and Harriman et al.

Like claim 1, claim 54 similarly calls for buffer memories, a multiple resource buffer and control circuit. Consequently, Applicants respectfully submit that the subject matter of claim 54 would not have been made obvious by the proposed combination of Chin et al. and Harriman et al.

With respect to claim 16, the office action alleges that this claim is "similar in scope to Claim 1, and therefore is rejected under the same rationale." 3/22/2006 Office Action, page 6. Claim 16 calls for a memory controller comprising a main processor related interface including read and write request queues; a first resource related interface including read and write request queues; a second resource related interface including read and write queues; and a multiple resource write request queue. Claim 1 does not specifically set forth such an arrangement of interfaces and read and write queues and Applicants respectfully submit that a generalized reference to claim 1 does not and cannot constitute a prima facie showing of the alleged obviousness of the subject matter of claim 16.

Moreover, neither Chin et al. nor Harriman et al. discloses, among other things, a multiple resource write request queue or a memory access control circuit that is coupled to receive read requests from the various read queues and write requests from the multiple resource write request queue. Consequently, the proposed combination of these documents is likewise deficient in this regard with respect to claim 16 and its dependent claims 17, 18 and 25.

These dependent claims contain features that provide additional bases for patentability.

By way of example without limitation, claim 25 requires that a resource that is writing to main memory generates a flush signal for initiating the flushing of that resource's write request queue. The office action contends that the "de-queuing" described at col. 13, lines 1-11 of Chin et al. discloses this feature. However, as noted above in the discussion of claim 14, this de-queuing operation is for queue 50c, which contains data whose source is the memory and whose destination is the processor. This queue is not a write request queue and there is no disclosure or suggestion in Chin et al. of initiating the flushing of a resource's write request queue when that resource is writing to main memory. For this additional and independent reason, claim 25 is believed to distinguish over the proposed combination of Chin et al. and Harriman et al.

With respect to claim 27, the office action alleges that "delaying forwarding requests for main memory access ..." and "granting requests ..." is "similar in scope to Claim 1 and is rejected under the same rationale." 3/22/2006 Office Action, page 7. Claim 1 does not specifically set forth such delaying or granting and Applicants respectfully submit that a

generalized reference to claim 1 does not and cannot constitute a prima facie showing of the alleged obviousness of the subject matter of claim 27.

Moreover, neither Chin et al. nor Harriman et al. disclose steps of storing requests in first and second queues and delaying forwarding requests as claimed and the office action identifies no portions of these references in support of its conclusion of obviousness. Consequently, Applicants respectfully submit that the proposed combination of Chin et al. and Harriman et al. would not have resulted in the subject matter of claim 27 or its dependent claims 28-30, 37, 39, 40, 43-46 and 53.

These dependent claims contain features that provide additional bases for patentability.

By way of example without limitation, claim 37 requires that a resource that is writing to main memory generates a flush signal for initiating the flushing of that resource's write request queue. The office action contends that the "de-queuing" described at col. 13, lines 1-11 of Chin et al. discloses this feature. However, as noted above in the discussion of claim 14, this de-queuing is with respect to queue 50c, which contains data whose source is the memory and whose destination is the processor. This queue is not a write request queue and there is no disclosure or suggestion in Chin et al. of initiating the flushing of a resource's write request queue when that resource is writing to main memory. For this additional and independent reason, claim 37 is believed to distinguish over the proposed combination of Chin et al. and Harriman et al.

With respect to claim 40, the office action states that this claim "is similar in scope to Claim 14, and therefore is rejected under the same rationale." 3/22/2006 Office Action, page 7. Here again, Applicants respectfully submit that a generalized statement of "similarity" to claim 14 does not constitute a prima facie showing of the alleged obviousness of claim 40. In any event, claim 40 requires generating a write queue flush signal by a first resource to initiate copying information in the first resource write request queue to main memory and flushing the first resource write request queue. In connection with claim 14, the office action references the de-queuing operation for queue 50c of Chin et al. as corresponding to the flushing of the write request queue. However, as explained above, queue 50c is involved with data read from memory 18 and the de-queuing operation is unrelated to flushing a write request queue as claimed. Consequently, claim 40 and its dependent claims 43-51 are not made obvious by the proposed combination of Chin et al. and Harriman et al.

These dependent claims contain features that provide additional bases for patentability.

Claims 8-12, 19-23, 31-35 and 47-51 were rejected under 35 U.S.C. Section 103(a) as allegedly being "obvious" over the proposed Chin et al-Harriman et al. combination, in view of Jeddeloh et al. (U.S. Patent No. 6,330,647). Applicants respectfully traverse this rejection.

Jeddeloh et al. was applied in connection with its alleged disclosure of an arbiter and control registers. However, even assuming that such features were somehow shown to be properly combinable with the result of the Chin et al.-Harriman et al. combination, Jeddeloh et al. does not remedy the deficiencies of Chin et al. and Harriman et al. with respect to claims 1, 16, 27 and 40, from which claims 8-12, 19-23, 31-35 and 47-51 depend.

The pending claims are believed to be in condition for allowance and favorable office action is respectfully requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 

Michael J. Shea
Reg. No. 34,725

MJS:mjs
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100